REMARKS

In the Office Action of March 23, 2004, the Examiner rejected claims 1-4 and 6, under 35 U.S.C. § 102(b) as being unpatentable over Japanese Patent Laid-Open Publication No. 8-125396 to Mitsuru (hereinafter, "Mitsuru"); and rejected claims 1-4, 6, and 7 under 35 U.S.C. § 103(a) as being unpatentable over Mitsuru in view of Japanese Patent Laid-Open Publication No. 7-211750 to Nagano et al. (hereinafter, "Nagano"). See Office Action, pgs. 2-3.

The Examiner's Rejection Under 35 U.S.C. §102(B) Should Be Withdrawn

Applicants respectfully traverse the rejection to claims 1-4 and 6, as being anticipated by Mitsuru. Anticipation under 35 U.S.C. § 102 requires that each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. If the prior art reference does not expressly set forth a particular element of the claim, that reference still may anticipate if that element is inherent in its disclosure. To establish inherency, the Office must show that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. (*See* M.P.E.P 2131 § (8th ed. 2001)).

Mitsuru is directed to mounting an electrical component to a substrate. (See Mitsuru, Purpose at page 1 of a certified English language translation of Mitsuru attached hereto for the Examiner's convenience). Specifically, Mitsuru aligns the electrical component (such as a BGA) to the substrate by aligning through holes formed on the electrical component with recognition marks formed on the substrate in order to

ensure that the balls of the BGA package are properly connected to the external lands of the substrate. *See* Mitsuru, paras. 0015-0017. Although, the "Patent Abstract" provided by the Examiner indicates that through holes 5 and 6 are bored in prescribed positions on a "main substrate 7," Applicants submit that this is obviously incorrect. If the holes and the recognition marks are both on the Mitsuru substrate, the user cannot view the recognition mark through the electrical component since no holes would be provided therethrough. In light of this apparent inconsistency Applicants obtained the attached certified English translation. The certified translation correctly indicates that the through holes are on electronic component 1, not on the substrate 7. *See* certified English language translation of Mitsuru, Structure at page 1 of the translation ("Each through hole in the electronic component . . . ." (emphasis added)). Moreover, the certified translation is confirmed by the Examiner's translated Patent Abstract, which provides at paragraph 0015 that "breakthroughs 5 and 6 are drilled in the electronic parts 1," not in substrate 7. In addition, the "Patent Abstract" provides that "[i]n the above configuration . . . alignment of the two tooling holes 5 and 6 drilled by the circuit board 2 of BGA 1 is carried out to the lands 8 and 9 to which the main substrate 7 corresponds, respectively." Patent Abstract of Mitsuru, para. 24. Therefore, the disclosure of "through holes 5 and 6 are bored in prescribed positions on a main substrate 7," in the "Constitution" section of the Patent Abstract is incorrect and does not accurately reflect the teachings of Mitsuru.

Thus, Mitsuru teaches forming breakthroughs in the electronic parts so as to allow the breakthroughs to show recognition marks on the substrate for proper positioning of the electronic part. Thus, Mitsuru does not disclose, either expressly or

inherently, all the elements of claim 1, including "forming a through hole from the back surface toward said conductive pattern," wherein the claimed "back surface" is part of the "substrate." Moreover, Mitsuru fails to teach of drilling holes of any kind and this is necessarily does not teach forming through holes "from a back surface" of the object, wherein a "conductive pattern" forming a "recognition mark" is formed on the front surface of that object.

Accordingly, Applicants respectfully request the Examiner to withdraw the rejection of claim 1, as well as claims 2-4 at least based on their dependency upon independent claim 1.

For the reasons set forth for the allowability of claim 1, claim 6, which contains similar claim limitations as claim 1, including "forming a through hole from the back surface toward said conductive pattern," is also allowable. Accordingly, Applicants respectfully request the Examiner to withdraw the rejection of claim 6 as well.

The Examiner's Rejection Under 35 U.S.C. § 103(a) Should Be Withdrawn

Applicants respectfully traverse the Examiner's rejection of claims 1-4, 6, and 7 under 35 U.S.C. § 103(a) as being obvious. To establish a *prima facie* case of obviousness, each of three requirements must be met. First, the references, taken alone or combined, must teach or suggest each and every element recited in the claims. (*See* M.P.E.P. § 2143.03 (8th ed. 2001)). Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the references in a manner resulting in the claimed invention. *See id.* Third, a reasonable expectation of success must exist. *See*

id. Moreover, each of the these requirements must "be found in the prior art, and not based on applicant's disclosure." (M.P.E.P. § 2143 (8th ed. 2001)).

As noted above, Mitsuru does not disclose, either expressly or inherently, all the elements of claim 1, including "forming a through hole from the back surface toward said conductive pattern," wherein the claimed "back surface" is part of the "substrate." Additionally, for these reasons, Mitsuru does not render claim 1 obvious. Moreover, Nagano does not overcome the deficiencies of Mitsuru.

The Examiner acknowledged that Nagano does not "suggest to form a through hole from a back surface of a surface of a substrate." (Office Action, pg. 4) and concedes that the through hole "is on the middle layer." *Id.* Since the through hole is not formed from a back surface, Nagano does teach or suggest "forming a through hole from the back surface toward said conductive pattern," wherein the claimed "back surface" is part of the "substrate."

In addition, the Examiner has provided no motivation to combine the references, nor a reasonable expectation of success. Applicants respectfully submit that the Examiner has apparently extracted items found in the prior art and combined them using Applicants' disclosure as improper hindsight without proper motivation to combine or a reasonable expectation of success. Such improper hindsight determinations are impermissible under 35 U.S.C. § 103.

Accordingly, Applicants respectfully request the Examiner to withdraw the rejection of claim 1, as well as claims 2-4 based on at least their dependency upon independent claim 1.

For the reasons set forth for the allowability of claim 1, claims 6 and 7, which contain similar claim limitations as claim 1, including "forming a through hole from the back surface toward said conductive pattern," are also allowable. Accordingly, Applicants respectfully request the Examiner to withdraw the rejection of claims 6 and 7.

CONCLUSION

In view of the foregoing amendments and remarks, Applicants respectfully request reconsideration and reexamination of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: June 23, 2004

By: _____
David L. Soltz
Reg. No. 34,731

Attachments: **Certification of Translation**
Certified Translation of Mitsuru

CERTIFICATION OF TRANSLATION

The undersigned, Richard Patner, whose address is 4809 Plummers Point Road Oshkosh, WI 54904, United States of America, declares and states as follows:

I am well acquainted with the English and Japanese languages; I have in the past translated numerous Japanese documents of legal and/or technical content into English.

I have been requested to translate into English the attached Japanese document titled **"Japanese Unexamined Patent Application Publication H08-125396 for an Electronic Component for mounting and method of mounting electronic component for mounting"** filed by Sony Corporation on October 26, 1994.

To a copy of this Japanese document I therefore attach an English translation and my Certification of Translation.

I hereby certify that the attached English translation of **"Japanese Unexamined Patent Application Publication H08-125396 for an Electronic Component for mounting and method of mounting electronic component for mounting"** filed by Sony Corporation on October 26, 1994 is, to the best of my knowledge and ability, an accurate translation.

And I declare further that all statements made herein of my own knowledge are true, that all statements made on information and belief are believed to be true, and that false statements and the like are punishable by fine and imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Richard Patner

June 23, 04
Date

[19] THE PATENT OFFICE OF JAPAN (JP)
[12] OFFICIAL GAZETTE FOR UNEXAMINED PATENTS (A)

[11] Disclosure Number 8-125396
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[54] [Title of Invention]

Electronic component for mounting and method of mounting electronic component for mounting

[57] [Summary]

[Purpose] The present invention provides an electronic component for mounting and a method of mounting an electronic component for mounting that facilitates the mounting alignment of an electronic component for mounting on a main substrate.

[Structure] Each through hole in the electronic component for mounting in question is aligned with a corresponding recognition mark on the main substrate so as to facilitate mounting alignment of the electronic component for mounting on the main substrate.

This provides an electronic component for mounting and a method of mounting an electronic component for mounting that enables the alignment of the main substrate with an electronic component for mounting, whose alignment could not be externally confirmed in the past, to be directly confirmed visually from above the electronic component for mounting in question.

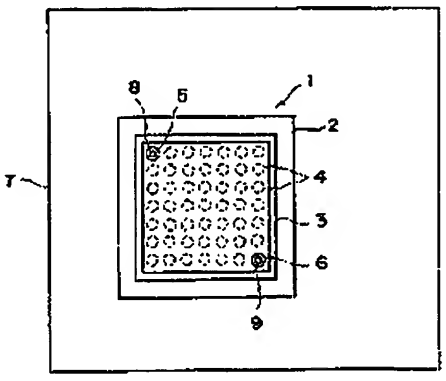

Figure 2. Mounting state of BGA relative to main substrate

[Scope of Patent Claim]

[Claim 1] An electronic component for mounting that is mounted at a prescribed position on a main substrate on which a prescribed wiring pattern is formed wherein through holes are bored in aforementioned electronic component for mounting at prescribed positions corresponding to at least two or more recognition marks that are formed at prescribed positions on aforementioned main substrate.

[Claim 2] The electronic component for mounting of Claim 1 provided with a mounting substrate on which a prescribed number of circuit elements are mounted, and with metal bumps formed on the opposite side of aforementioned mounting substrate from the surface on which is mounted each of aforementioned circuit elements so as to conduct and connect with a prescribed quantity of wiring that is drawn from each of aforementioned circuit elements, said bumps positioned corresponding to aforementioned wiring pattern on aforementioned main substrate.

[Claim 3] The electronic component for mounting of Claim 2 in which each of aforementioned through holes for aforementioned electronic component for mounting is established on the outer edge on diagonal lines of sites corresponding to desired metal bumps from among each of aforementioned metal bumps on aforementioned mounting substrate.

[Claim 4] The electronic component for mounting of Claim 2 in which prescribed transparent material is embedded in each of aforementioned through holes of aforementioned electronic component for mounting and in which prescribed calibration is plotted in all aforementioned transparent material.

[Claim 5] The electronic component for mounting of Claim 2 in which the hole diameter of each of aforementioned through holes in aforementioned electronic component for mounting is made somewhat larger than the outer diameter of aforementioned metal bumps.

[Claim 6] A method of mounting electronic components for mounting in which electronic components for mounting are mounted at prescribed positions on a main substrate on which a prescribed wiring pattern is formed, wherein

at least two or more recognition marks are formed at prescribed positions on aforementioned main substrate,

through holes are bored in aforementioned electronic component for mounting at positions corresponding to aforementioned recognition marks,

aforementioned electronic components for mounting are aligned with aforementioned main substrate based on each of aforementioned recognition marks and on the spatial relationship of each of aforementioned through holes with each of aforementioned recognition marks when aforementioned electronic components for mounting are mounted on aforementioned main substrate.

[Claim 7] The method of mounting electronic components for mounting of Claim 6 in which aforementioned electronic components for mounting have a mounting substrate on which are mounted a prescribed number of circuit elements, and have metal bumps formed on the opposite side of aforementioned mounting substrate from the surface on which is mounted each of aforementioned circuit elements so as to conduct and connect with a prescribed quantity of wiring that is drawn from each of aforementioned circuit elements, said bumps positioned corresponding to aforementioned wiring pattern on aforementioned main substrate.

[Claim 8] The method of mounting electronic components for mounting of Claim 7 in which each of aforementioned through holes for aforementioned electronic component for mounting is established on the outer edge on diagonal lines of sites corresponding to desired metal bumps from among each of aforementioned metal bumps on aforementioned mounting substrate.

[Claim 9] The method of mounting electronic components for mounting of Claim 7 in which prescribed transparent material is embedded in each of aforementioned through holes of aforementioned electronic component for mounting and in which prescribed calibration is plotted in all aforementioned transparent material.

[Claim 10] The method of mounting electronic components for mounting of Claim 7 in which the hole diameter of each of aforementioned through holes in aforementioned electronic component for mounting is made somewhat larger than the outer diameter of aforementioned metal bumps.

[Detailed Description of the Invention]

[0001]

[Contents] The present invention is explained in the following sequence.

Field of Industrial Utilization

Related Art
Problems Solved by the Invention
Means of Solving the Problems (Figure 1 to Figure 4)
Action (Figure 1 to Figure 4)
Embodiments (Figure 1 to Figure 4)
Effects of Invention

[0002]

[Field of Industrial Utilization] The present invention concerns an electronic component for mounting and a method of mounting an electronic component for mounting. It is ideally applied, for example, to an electronic component for mounting and a method of mounting an electronic component for mounting wherein semiconductor chips are sealed within a package.

[0003]

[Related Art] A past example of such an electronic component for mounting is a ball grid array (BGA) in which a prescribed number of metal bumps are positioned in lattice form as terminals for external connection on the reverse side (specifically, junction plane with a main substrate) of a package of sealed semiconductor elements.

[0004] Specifically, a BGA is established with a circuit substrate structured with signal lines comprising conductors such as silver or copper wired in a prescribed pattern on the surface of a foundation in which inorganic material such as ceramic or organic material such as glass epoxy serves as an insulation layer.

[0005] On the other hand, semiconductor elements are die bonded on the other side of the BGA foundation. Electrode terminals of the semiconductor elements in question and electrode elements of the circuit substrate are wire bonded via through holes, specifically, they are connected via metal wires of gold, for example, followed by protection of the semiconductor elements in question by overcoating with resin such as epoxy or by covering with a cap of metal, etc.

[0006] In this case, a prescribed number of signal wires drawn from the semiconductor elements form circuit wiring with a prescribed pattern on the opposite side of a package via through holes. Furthermore, lands are established in the circuit wiring in question to electrically connect on the outside of the main substrate (mother board). A prescribed number of metal balls corresponding to the lands in question are connected using solder or a prescribed number of metal balls of solder are directly connected to form ball electrodes.

[0007] Here, a plurality of circuit substrates must be laminated to form multiple layers upon increase in the number and density of signal wires drawn from the semiconductor elements to the circuit substrate. Consequently, when increasing the layers by sequential lamination of circuit substrates, the insulation layer and the layer having circuit wiring are laminated so as to be mutually interposed, followed by connecting these layers via a plurality of through holes established in the respective circuit substrates to complete the connection of the electrode terminals of the semiconductor elements with the lands on the opposite side of the package.

[0008] When the circuit substrate of such a BGA is electrically connected externally with the main substrate, the lands of the external main substrate are relatively aligned with a prescribed number of ball electrodes that are positioned via a prescribed pattern on the circuit substrate of the BGA in question, followed by joining via reflow soldering.

[0009] A concrete proposal to mount a BGA on a main substrate has been to center a BGA via a mechanical chuck of an automatic component mounting device (not illustrated), followed by indirectly aligning it relative to the lands of the main substrate. An additional mounting proposal has been to mount a BGA on a main substrate by calculating the center of the BGA in question using a visual recognition device (not illustrated) based on the external BGA configuration, followed by indirectly aligning it with the lands on the outside of the main substrate based on the results of such calculation.

[0010]

[Problems Solved by the Invention] However, the aforementioned methods present difficulties, including the inability of the operator to confirm the spatial relationship of the external lands of the main substrate relative to each ball electrode of the BGA when aligning the ball electrodes formed in each electrode terminal of the circuit substrate of the BGA relative to the external lands of the main substrate.

[0011] A method of confirming the spatial relationship of the BGA relative to the external main substrate via a transmission image formed by X-ray beam irradiation has been proposed. However, when the BGA

circuit substrate or external main substrate comprise a number of layers, confirmation of the position of each ball electrode and of the position of each land of the main substrate corresponding thereto is difficult for the operator since the operator sees those layers superimposed, and the results remain inadequate.

[0012] Another method of resolving such problems has been to try to confirm only the alignment by using a structure comprising only electrode elements and ball electrodes rather than multiple layers of BGA circuit substrates as a so-called mechanical sample. However, the problem persists unresolved of the operator seeing laminates of these layers with the external main substrate remaining in multiple layers.

[0013] The present invention was devised in light of aforementioned points. It proposes an electronic component for mounting and a method of mounting an electronic component for mounting that facilitates mounting alignment of electronic components for mounting relative to the main substrate.

[0014]

[Means of Solving the Problems] The present invention that resolves such problems has through holes 5, 6 established in electronic component 1 for mounting at prescribed positions corresponding to at least two or more recognition marks 8, 9 that are formed at prescribed positions on main substrate 7, said electronic component 1 being mounted at a prescribed position on main substrate 7 in which a prescribed wiring pattern is formed.

[0015] Furthermore, in the method of mounting electronic component 1 at a prescribed position on main substrate 7 in which a prescribed wiring pattern is formed in the present invention, at least two or more recognition marks 8, 9 are formed at prescribed positions on main substrate 7. Through holes 5, 6 are bored in electronic component 1 for mounting that corresponds to each recognition mark 8, 9, and electronic component 1 for mounting is aligned relative to main substrate 7 based on each recognition mark 8, 9 as well as on the spatial relationship of each through hole 5, 6 corresponding to each recognition mark 8, 9 when mounting electronic component 1 for mounting on main substrate 7.

[0016] Furthermore, in the present invention, electronic component 1 for mounting is provided with mounting substrates 2, 3 on which a prescribed number of circuit elements are mounted, and with metal bumps 4 formed on the opposite side of aforementioned mounting substrates 2, 3 from the surface on which is mounted a prescribed number of circuit elements so as to conduct and connect with a prescribed quantity of wiring that is drawn from each of the circuit elements, said bumps positioned corresponding to the wiring pattern on main substrate 7.

[0017]

[Action] When electronic component 1 for mounting is mounted on main substrate 7, the mounting alignment of electronic component 1 for mounting relative to main substrate 7 can be easily confirmed by aligning each through hole 5, 6 of the electronic component 1 for mounting in question with the corresponding recognition marks 8, 9 on main substrate 7.

[0018]

[Embodiments] Embodiments of the present invention are explained in detail below with reference to the appended figures.

[0019] In Figure 1, reference numeral 1 denotes a BGA overall. The semiconductor elements in question are packaged by overcoating semiconductor elements (not illustrated) that are die bonded on the surface of mounting substrate 2 with sealing material 3 comprising epoxy resin, for example.

[0020] In addition, a prescribed number of signal wires (not illustrated) drawn from this semiconductor element are connected via through holes (not illustrated) to the electrode elements (not illustrated) that are positioned in a prescribed pattern on the opposite side of circuit substrate 2. Furthermore, ball electrode terminal 4 is formed by joining solder balls corresponding to the electrode elements in question. In this case, circuit substrate 2 is formed in a virtually square plate shape, and ball electrode terminals 4 on the surface of the circuit substrate 2 in question are established in a prescribed pattern equal in number to each column and row in lattice form.

[0021] Here, in BGA 1, orientation holes 5 and 6 are made somewhat larger than the outer diameter of the ball electrode terminals 4 in question without establishing ball electrode terminals 4 at two edge sites (below termed (diagonal edge sites) on a diagonal line from the center of ball electrode terminals 4 arrayed in lattice form on the surface of circuit substrate 2. Thus, an operator can confirm any shifting of position between the orientation holes 5, 6 in question and the lands of the corresponding main substrate by viewing the main substrate (not illustrated) through orientation holes 5, 6 bored in BGA 1.

[0022] In practice, when boring two orientation holes 5 and 6, the operator aligns two diagonal edge sites in circuit substrate 2 and in sealing material 3 of BGA 1 using a tool (not illustrated) that opens holes, such as a drill, after completing the BGA 1 production step. At that time, the operator first aligns the central positions of two diagonal edge sites (specifically, the central positions of ball electrode terminals 4 installed at the sites in question) with the central positions of orientation holes 5 and 6 so as to match, and then bores through circuit substrate 2 from the side having ball electrode terminals 4. In addition, the operator then irradiates an X-ray beam to confirm the positions of two diagonal edge sites of ball electrode terminals 4, followed by boring through mounting substrate 2, 3 from the side lacking ball electrode terminals 4.

[0023] When selecting the hole diameter of orientation holes 5 and 6, the operator cannot confirm the occurrence of any shifting that occurs if the hole diameter of orientation holes 5 and 6 is somewhat smaller than the outer diameter of ball electrode terminals 4 (hereinafter abbreviated ball diameter) since it would be equal to or somewhat smaller than the size of the land of circuit substrate 2. On the other hand, if the hole diameter of orientation holes 5 and 6 is excessively larger than the ball diameter, that would interfere with other adjacent ball electrode terminals 4, in which case the operator would be unable to confirm the existence of any shifting. This problem is resolved by boring hole diameters of orientation holes 5 and 6 that are somewhat larger than the ball diameter. Specifically, if the ball diameter of ball electrode terminals 4 is 0.8 [mm], the hole diameter of orientation holes 5 and 6 should be 1.2 [mm].

[0024] In aforementioned structure, two orientation holes 5 and 6 bored in circuit substrate 2 of BGA 1 are aligned with lands 8 and 9 that match main substrate 7 when mounting each ball electrode terminal 4 of BGA 1 on a land matching main substrate 7, as shown in Figure 2.

[0025] The orientation states of two orientation holes 5 and 6 bored in circuit substrate 2 of BGA 1 and in sealing material 3, and of lands 8 and 9 of main substrate 7 corresponding to the orientation holes 5 and 6 in question are shown in Figure 3. First, when two orientation holes 5 and 6 bored in circuit substrate 2 of BGA 1 are precisely aligned with lands 8 and 9 corresponding to main substrate 7, the centers of orientation holes 5 and 6 in question and of the corresponding lands 8 and 9 are positioned concentrically (Figure 3 (A)).

[0026] Then, if two orientation holes 5 and 6 bored in circuit substrate 2 of BGA 1 are not precisely aligned with lands 8 and 9 corresponding to main substrate 7, the centers of the orientation holes 5 and 6 in question and the centers of the corresponding lands 8 and 9 will deviate by prescribed distance w in a prescribed direction (hereinafter termed amount of deviation) (Figure 3 (B)).

[0027] Thus, the amount of deviation w in question can be measured using a measurement apparatus such as a microscope or projector, and the mounting position of BGA 1 can be corrected based on the measurement results in question, thereby allowing BGA 1 to be precisely positioned on main substrate 7. Furthermore, the direction of amount of deviation of BGA 1 relative to main substrate 7 can be measured not only in the X axial- and Y axial-directions but the amount of deviation even in the rotational direction can be measured since the amount of deviation w is measured at two sites.

[0028] Individual ball electrode terminals 4 of BGA 1 can be mounted in corresponding lands on main substrate 7 by boring orientation holes 5 and 6 that are somewhat larger than the external shape of ball electrode terminals 4 at two diagonal edge sites from the centers of ball electrode terminals 4 arrayed in lattice shape on the surface of circuit substrate 2 of BGA 1 in aforementioned structure. The relative positions of the orientation holes 5 and 6 in question and of the corresponding lands 8 and 9 can then be easily confirmed. In this way, the alignment of BGA 1 and main substrate 7, which could not be confirmed externally in the past, can now be directly confirmed visually from above BGA 1.

[0029] Aforementioned embodiment discusses the establishment of orientation holes 5 and 6 at two diagonal edge sites on the surface of circuit substrate 2 in BGA 1, but the present invention is not restricted to this. As shown in Figure 4, the present invention can also be applied to the embedding of transparent epoxy resin with prescribed section calibrations plotted thereupon (hereinafter abbreviated calibration window) 10 and 11 in surface sections of aforementioned orientation holes 5 and 6.

[0030] In this case, the same effects as those mentioned above can be realized by aligning calibration windows 10 and 11 installed on circuit substrate 2 of BGA 1 with corresponding lands 8 and 9 of main substrate 7 after mounting each ball electrode terminal 4 of BGA 1 on lands corresponding to main substrate 7.

[0031] In short, when establishing calibration windows 10 and 11, the BGA 1 is first produced, after which the operator bores two orientation holes 5 and 6 in circuit substrate 2 and sealing material 3 of BGA 1 using an apparatus for opening a hole, such as a drill (not illustrated). Next, transparent epoxy resin is poured into the orientation holes 5 and 6 in question and solidified, followed by laser light irradiation of prescribed section calibrations from the surface of circuit substrate 2 having ball electrode terminals 4 using a prescribed laser device (not illustrated), thereby permitting the central positions of orientation holes 5 and 6 to be plotted to a standard. For example, this prescribed section calibration would be line width of 0.01 [mm] and calibration pitch of 0.1 [mm]. Furthermore, the operator could visually confirmed the alignment every easier through plotting aforementioned section calibration by applying dye.

[0032] Aforementioned embodiment discusses the case in which orientation holes 5 and 6 are established at two edge sites having a diagonal spatial relationship on a given diagonal line from the centers of ball electrode terminals 4 arrayed in lattice shape on the surface of circuit substrate 2 of BGA 1, but the present invention is not restricted to this relationship. Orientation holes may be established at prescribed sites having ball electrode terminals 4 other than at the edge sites in question, and the number of orientation holes, rather than being restricted to two, may be three or more.

[0033] Aforementioned embodiment discusses the case in which orientation holes 5 and 6 are established at two edge sites having a diagonal spatial relationship on a given diagonal line from the centers of ball electrode terminals 4 arrayed in lattice shape on the surface of circuit substrate 2 of BGA 1, but the present invention is not restricted to this relationship. The present invention may be applied to the establishment of one or two orientation holes at two edge sites having a diagonal spatial relationship on another diagonal line in addition to the orientation holes 5 and 6 in question.

[0034] Aforementioned embodiment discusses the boring of orientation holes 5 and 6 through circuit substrate 2 and sealing material 3 of BGA 1, but the present invention is not restricted to this. When boring orientation holes at prescribed sites having ball electrode terminals 4 arrayed on the surface of circuit substrate 2, if holes perforate only circuit substrate 2 without perforating sealing material 3, the present invention may be applied to the boring of orientation holes at the sites in question.

[0035] Furthermore, aforementioned embodiment discusses the boring of orientation holes at prescribed sites on ball electrode terminals 4 arrayed on circuit substrate 2, but the present invention is not restricted to this. Orientation holes may be established at prescribed sites other than at sites having ball electrode terminals 4 on the surface of circuit substrate 2.

[0036] In this case, alignment marks may be made at prescribed positions on main substrate 7 corresponding to a prescribed number of orientation holes bored in circuit substrate 2 when precisely aligning each ball electrode terminal 4 of BGA 1 on lands corresponding to main substrate 7. By so doing, the operator can attain the same effects as those noted above by easily confirming the relative positions of the orientation holes and of the corresponding marks.

[0037]

[Effects of Invention]

In the present invention discussed above, an electronic component for mounting on a main substrate can be easily mounted and aligned by aligning each perforation hole of the electronic component for mounting in question with a corresponding recognition mark on the main substrate when mounting an electronic component for mounting on a main substrate. Thus, the present invention provides a method of mounting an electronic component for mounting in which the alignment state with the main substrate of the electronic component for mounting, which could not be confirmed externally in the past, can be directly confirmed visually from above the electronic component for mounting in question.

[Brief Description of Drawings]

[Figure 1] A perspective diagram showing a BGA in one embodiment of the present invention.

[Figure 2] A planar figure showing the mounting state of a BGA on a main substrate in the present invention.

[Figure 3] A partial planar figure showing the alignment state of the BGA and the main substrate in the present invention.

[Figure 4] A partial planar figure showing the alignment state of the BGA and the main substrate in another embodiment.

[Explanation of Notations]

1.. BGA, 2.. circuit substrate, 3.. sealing material, 4.. ball electrode terminal, 5, 6.. orientation holes, 7.. main substrate, 8, 9.. lands, 10, 11.. calibration windows

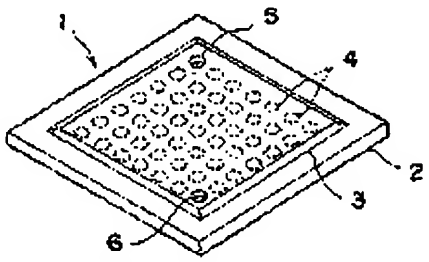

Figure 1 Structure of an embodiment

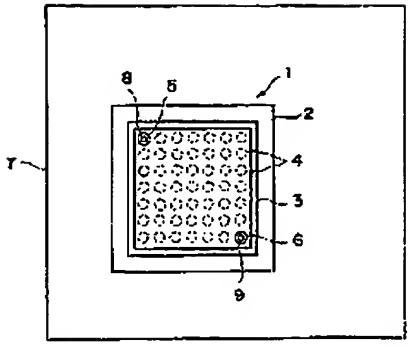

Figure 2. Mounting state of BGA relative to main substrate

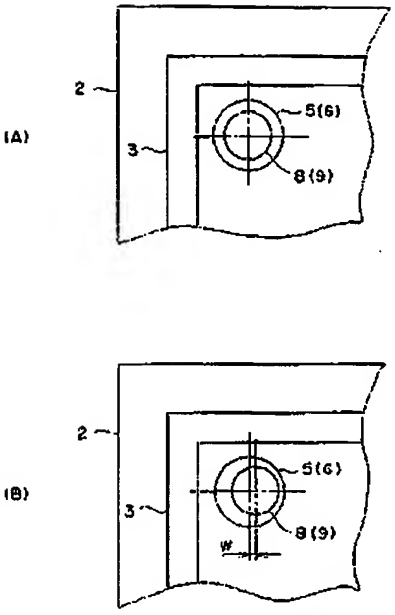

Figure 3. Alignment state of BGA relative to main substrate

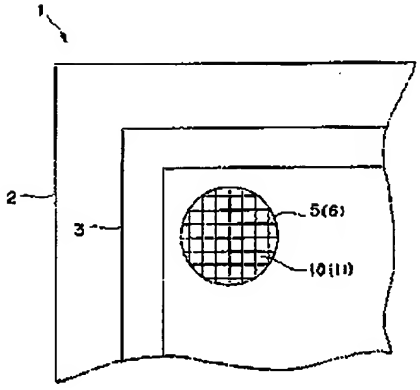

Figure 4. Another embodiment